

TDA8102B

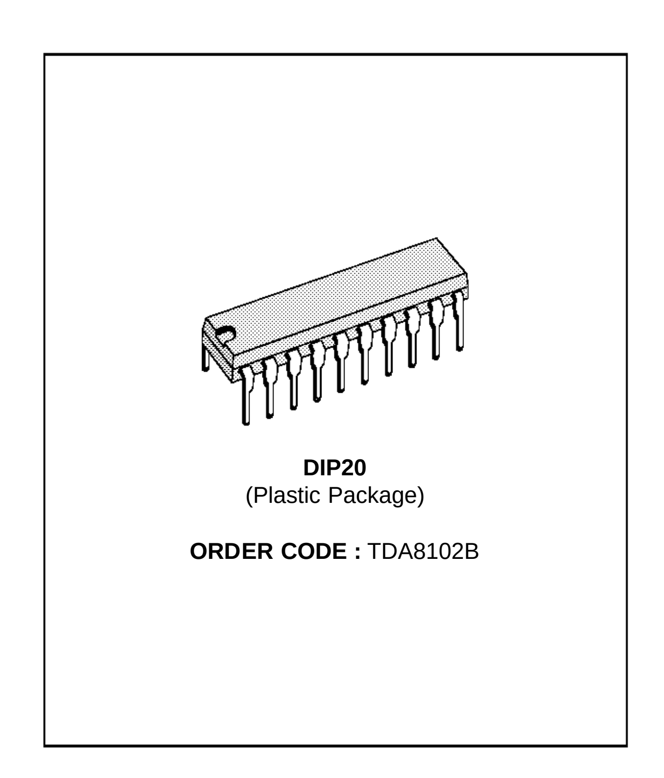
H/V PROCESSOR FOR TTL V.D.U

HORIZONTAL SECTION

- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 15kHz to 100kHz
- HORIZONTAL OUTPUT PULSE SHAPER AND SHIFTER
- PHASE COMPARATOR BETWEEN SYNCHRO AND OSCILLATOR (PLL1)
- PHASE COMPARATOR BETWEEN FLYBACK AND OSCILLATOR (PLL2)
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR PHASE AND FREQUENCY

VERTICAL SECTION

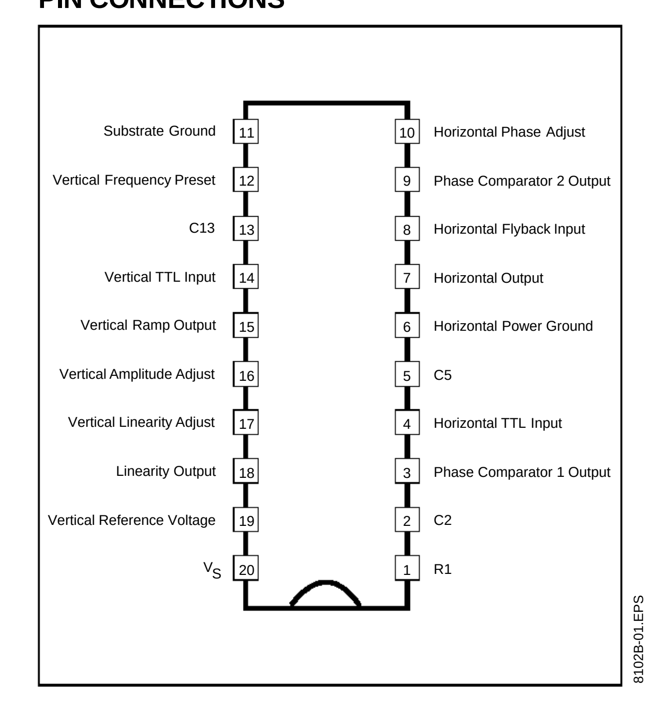
- SYNCHRONIZATION INPUT : TTL COMPATIBLE, NEGATIVE EDGE TRIGGERED
- SYNCHRONIZATION INDEPENDENT FROM DUTY CYCLE TIME
- OSCILLATOR : FREQUENCY RANGE FROM 30Hz to 120Hz
- RAMP GENERATOR WITH VARIABLE GAIN STAGE
- VERTICAL RAMP VOLTAGE REFERENCE
- INTERNAL VOLTAGE REGULATOR
- DC COMPATIBLE CONTROLS FOR FREQUENCY, AMPLITUDE AND LINEARITY



DIP20
(Plastic Package)

ORDER CODE : TDA8102B

PIN CONNECTIONS

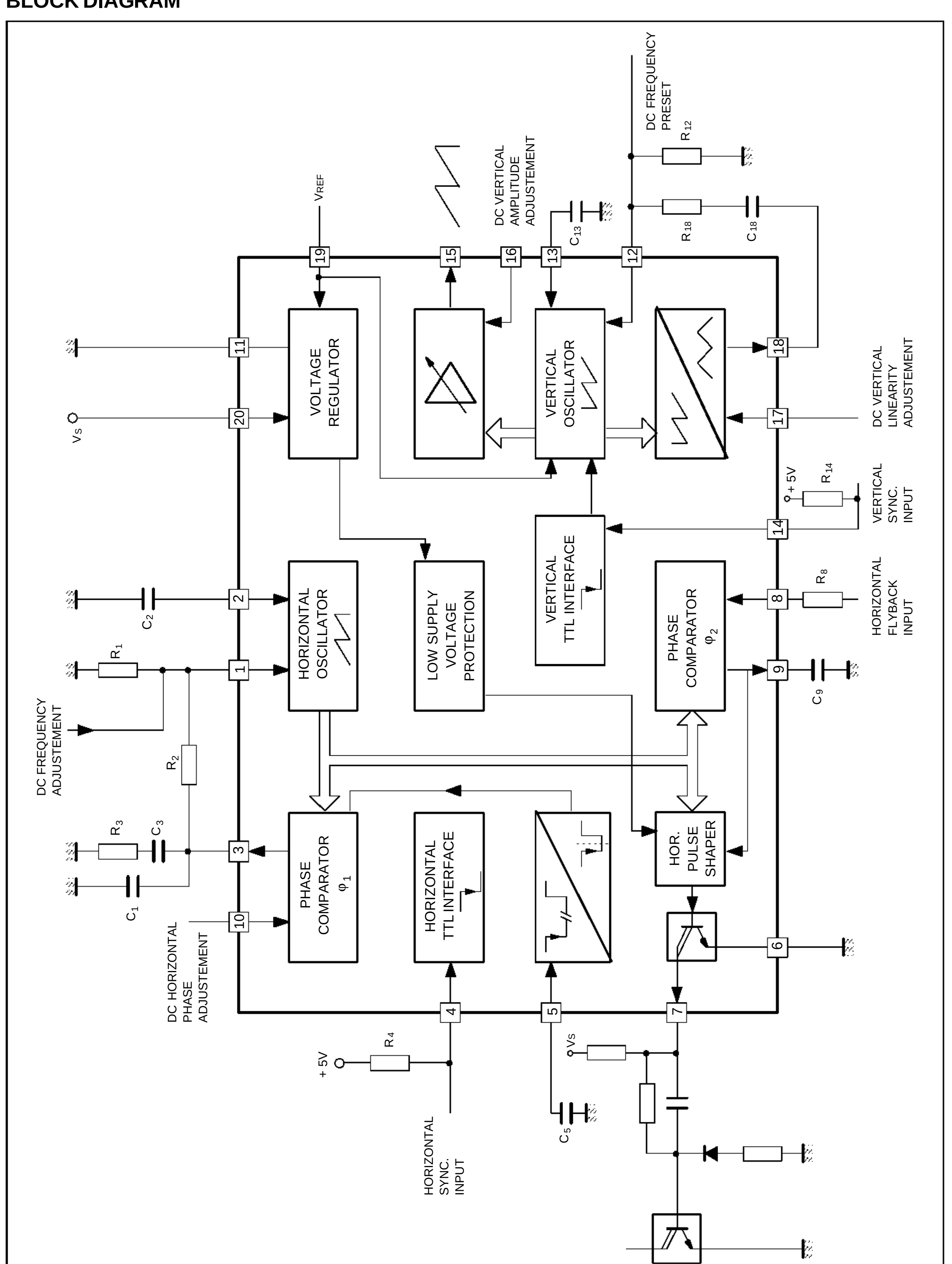


DESCRIPTION

The TDA8102B is a monolithic integrated circuit for horizontal and vertical sync processing in monochrome and color video displays driven by input TTL compatible signals.

The TDA8102B is supplied in a 20 pin dual in line package with pin 11 connected to ground and used for heatsinking.

BLOCK DIAGRAM



SGS-THOMSON MICROELECTRONICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	18	V
V_{SYNC}	Sync Input Peak Voltage	+ V_S	V
I_{OH}	Output Sinking Peak Current (Pin 7 ; t < 3µs)	2	A
I_{15}	Output current (Pin 15)	- 10	mA
I_{19}	Output Current (Pin 19)	- 10	mA
P_{TOT}	Total Power Dissipation Tamb < 70°C T_{pin} < 90°C	 1.4 1.5	 W W
T_{STG} , T_J	Storage and Junction Temperature	- 40, +150	°C

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THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(J-C)}$	Junction-case Thermal Resistance	40	°C/W
$R_{TH(J-A)}$	Junction-ambient Thermal Resistance	55	°C/W

8102B-02.TBL

ELECTRICAL CHARACTERISTICS

(T_{AMB} = 25°C, V_S = 12V, refer to the test circuits, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
HORIZONTAL SECTION						
V_S	Supply voltage range		10.5	12	15.5	V
I_S	Supply current			50	70	mA
V_1	Voltage reference at Pin 1	I_1 = 0.5mA	3.2	3.5	3.8	V
I_1	Current at Pin 1		- 1			mA
V_2	Voltage swing at Pin 2			4		V_{PP}
K_0	Free running frequency constant	$f_o = 1/(K_0 \times R1 \times C2)$	2.8	3.04	3.2	
$\lvert V_3 - V_1 \rvert$	Control voltage range	(See technical note 1)		2.5		V
$\lvert I_3 \rvert$	Peak control current			3		mA
K_3	Gain phase comparator φ1 $K_3 = 2 \times I_3 /360$			16.6		$\frac{\mu A}{degree}$
V_4	Sync threshold input (neg. edge)	Sync high Sync low	2		8 0.8	V V
I_4	Current at Pin 4	Input high Input low	 - 10		10	µA µA
T_4	Input pulse duration $T = 1/f_H$		1		0.9T	µs
V_5	Monostable threshold		5.7	6	6.3	V
t_5	Internal pulse width $t_5 = C5 \times V_5 / I_5$	C5 = 220 pF (see technical note 2)		3.6		µs
t_7	Output pulse duration (low) - $T = 1/f_H$	@ f_H = 27 kHz @ f_H = 100 kHz		0.33T 0.25T		µs µs
V_7 sat	Output Saturation Voltage	I_7 = 600 mA		1.2	2.5	V
t_D	Permissible delay between output pulse leading edge and flyback pulse leading edge (for keeping a constant duty cycle) ; $T = \frac{1}{f_H}$	See technical note 4		0.30 T - t_{FLY}		s
V_{FLY}	Flyback threshold voltage at Pin 8		0.6	0.7	0.9	V
I_{FLY}	Flyback input current at Pin 8	Flyback On Flyback Off	0.6 -1		2	mA mA
V_8	Clamp voltage at Pin 8	I_8 = 1mA I_8 = - 1mA	0.6		 - 0.6	V V
I_8	Current for switching low the output pulse		0.7		2	mA

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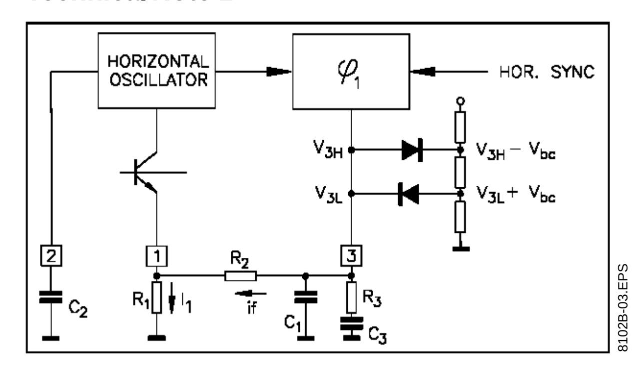
ELECTRICAL CHARACTERISTICS

(T_{AMB} = 25^oC, V_S = 12V, refer to the test circuits, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
HORIZONTAL SECTION						
K_9	Phase sensitivity at Pin 9	(See technical note 3)		67.5		$\frac{degree}{V}$
V_{10}	Control voltage range		0.5		4.5	V
K_{10}	Phase control sensitivity at Pin 10		20	22.5	30	$\frac{degree}{V}$
	Horizontal phase adjustment	Zero degree phase: flyback centered on the center of the pulse at Pin 5	- 45		+ 45	degree
K_1	Phase jitter constant (jitter = $\frac{K_1}{10^6 \ . \ f_H}$)			100	150	ppm
K_2	Frequency drift versus supply voltage $K_2 = \frac{dF \ . \ 10^6}{dV \ . \ f_H}$	V_S = 10.5V to 15.5V			2000	$\frac{ppm}{V}$
VERTICAL SECTION						
V_{12}	Voltage reference at Pin 12		3.2	3.5	3.8	V
$\frac{I_{13}}{I_{12}}$	Current gain at Pin 13			1		
V_{13}	Vertical ramp amplitude			4		V_{PP}
t_{FALL}	Discharge time at Pin 13	C_{18} = 0.22 µF V_{13} = $4V_{PP}$		10	22	µs
K_{14}	Synchro window constant $t_s = \frac{K_{14}}{f_V}$	(See technical note 6)		0.333		
V_{14}	Sync input threshold (negative edge)	• Sync high • Sync Low	2		8 0.8	V V
I_{14}	Current at Pin 14	• Input high • Input Low	 - 10		10	µA µA
t_{14}	Input pulse duration $T = \frac{1}{f_V}$		10		0.5T	µs
V_{15}	Average value of voltage on Pin 15	V_{13} = $4V_{PP}$ V_{16} = 2.5V		4		V
$\lvert I_{15} \rvert$	Output current at Pin 15				1	mA
K_{15}	Buffer gain constant at Pin 15 $V_{15PP} = K_{15} \ . \ V_{13PP}$	V_{16} = 2.5V		1		
K_{16}	Buffer variable gain constant at Pin 15 $K_{16} = \frac{\Delta V_{15PP}}{\Delta V_{16} \ . \ V_{13PP}}$	2.5V < V_{16} < 4.5V 0.5V < V_{16} < 2.5V		0.1		V^{-1}
I_{16}	Input bias current at Pin 16	V_{16} = 0.5V	- 50			µA
I_{17}	Input bias current at Pin 17	V_{17} = 4.5V			50	µA
V_{18}	Average voltage at Pin 18 : $V_{18} = 2 + \frac{V_{18PP}}{2}$	V_{17} = 3.5V R_{18} not connected		3		V
K_{18}	Linearity correction constant $K_{18} = \frac{\Delta V_{18PP}}{\Delta V_{17}}$	V_{13PP} = 4V, 1.5V < V_{17} < 4.5V		1		
V_{19}	Voltage reference at Pin 19	(See technical note 5)	7.6	8	8.2	V
$\lvert I_{19} \rvert$	Current at Pin 19				2	mA
K_{17}	Frequency drift versus supply voltage $K_{17} = \frac{dF \ . \ 10^6}{dV \ . \ f_V}$	V_S = 10.5V to 15.5V			4500	$\frac{ppm}{V}$

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Technical Note 1



$f_{H\ (nom)}$ = 26.8 kHz

R1 = 6.8k Ω

R2 = 56 kΩ

C2 = 1.8 nF

$$f_{pull\text{-}in} = f_{H\ (nom)} \frac{|V_3 - V_1| / R2}{V_1 / R1} = f_{H\ (nom)} \frac{I_f}{I_o} \qquad (A)$$

where: V_1 = 3.5V and $|V_3 - V_1|$ is the control voltage range.

The voltage at Pin 3 is limited by two clamping diodes at the voltage V_{3H} and V_{3L}.

When the PLL1 is synchronized and perfectly tuned, $V_3 = V_1$.

Remark: The value of C2 influences the horizontal oscillator free running frequency; it doesn't effect the pull-in range. If the horizontal frequency is changed by using R1, the pull-in range changes accordingly with the formula (A).

Technical Note 2

The internal pulse "t_5", is generated by the current generator "I_5" charging the external capacitor "C5", according with the formula (B):

$$t_5 = \frac{C5\ .\ V_5}{I_5} \quad (B),\ t_5 = \frac{T_H}{12} \quad \text{is recommended.}$$

Technical Note 3

K_9 = 67.5 degrees/volt represents the slope of the oscillator charging period of the waveform at Pin 2:

$$K_9 = \frac{360 \times 0.75}{4} \quad \frac{degree}{V}$$

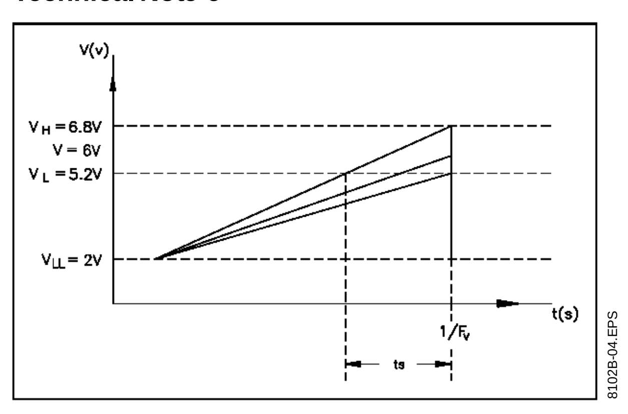
Technical Note 4

The second PLL can recover the storage of horizontal output stage maintaining a constant duty cycle till the trailing edge of the output pulse gets the trailing edge of the flyback pulse. From this point on, only the leading edge of the output pulse will be shifted covering a total phase shift of: 0.30T; overcoming this value, it will produce a notch in the output pulse (@ f_H = 27kHz).

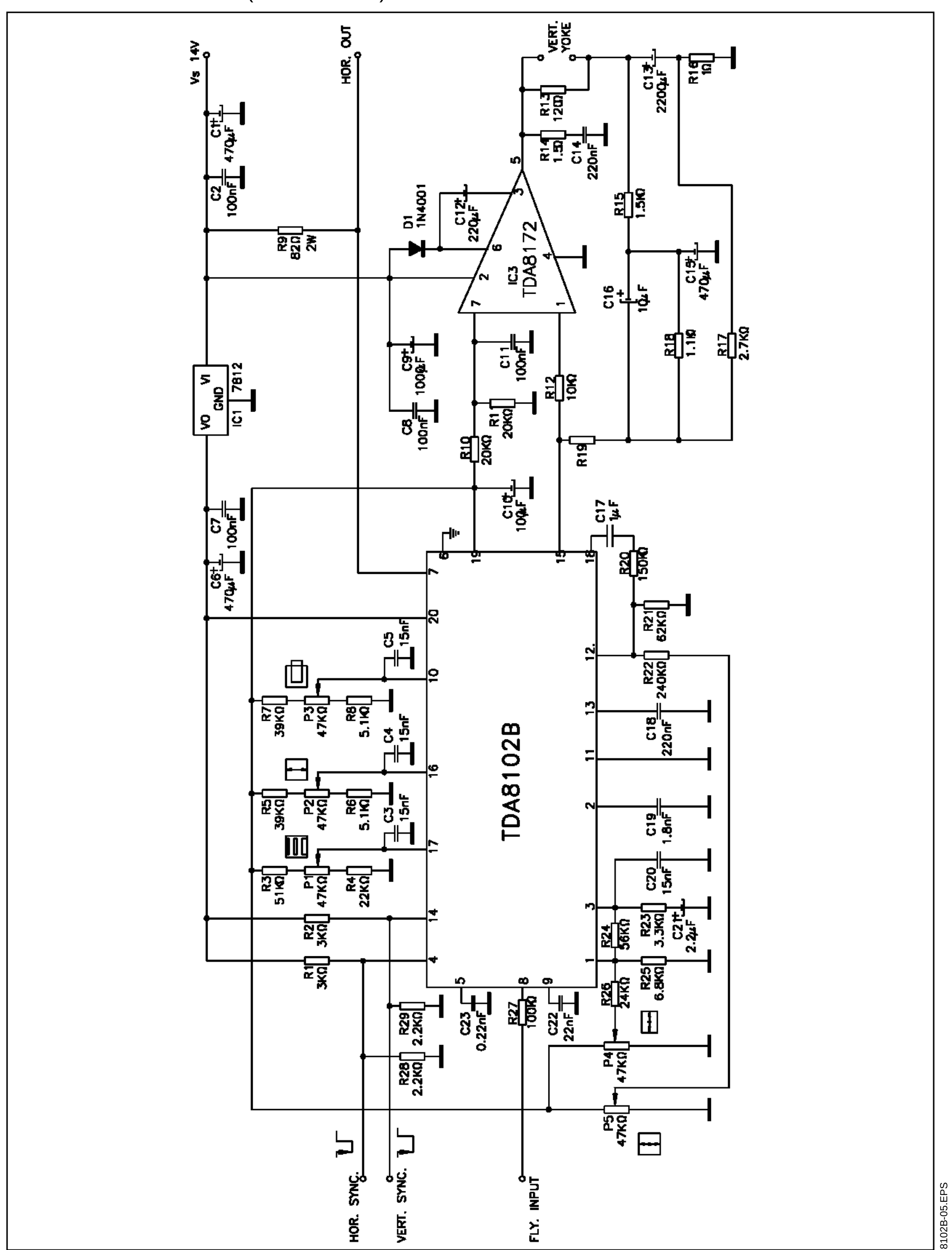
Technical Note 5

The voltage reference at Pin 19 can be used to polarize the DC operating point of the vertical booster. This voltage corresponds to the double of the mean value voltage of the vertical sawtooth at Pin 13.

Technical Note 6



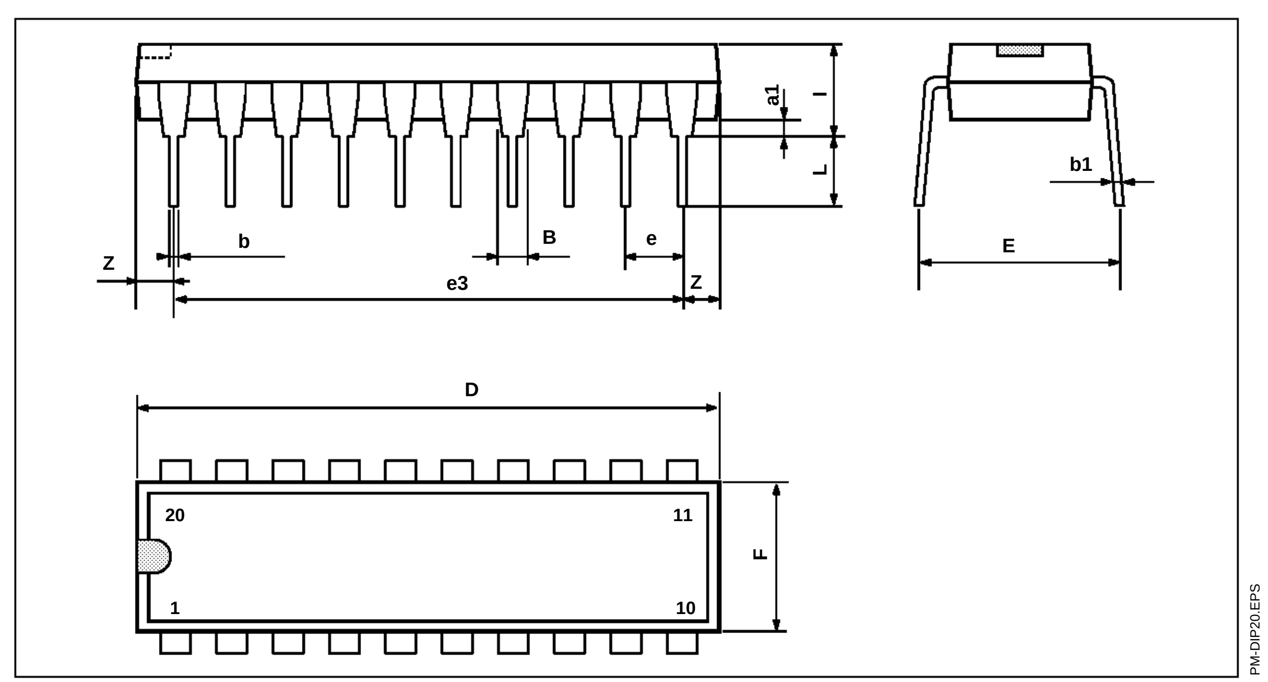
APPLICATION DIAGRAM (with TDA8172)



8102B-05.EPS

PACKAGE MECHANICAL DATA

20 PINS - PLASTIC DIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
i			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

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